Patent claims

1. An electrical test circuit for testing integrated circuits, particularly dynamic A/D converters, the electrical test circuit (5) comprising the following features:

- a first input (51) which is intended for receiving a test signal of an integrated circuit (4),
- a second input (52), which is intended for receiving a control signal,
- a third input (53) which is adapted to receive a normalized reference signal, particularly one that is formed to be synchronous with the test signal,
- a control device (55) which is constructed in such a manner that the deviation and/or the amplitude and/or the phase of the reference signal and/or of the test signal is or, respectively, are changed,
- a measuring device (56) which is constructed in such a manner that a difference signal is generated by subtracting the reference signal from the test signal,
- an output (54) which is intended for outputting the difference signal.

2. The electrical test circuit according to claim 1, characterized in that the measuring device (55) is constructed in such a manner that at least one quality parameter is generated from the difference signal, the output (54) being intended for outputting the difference signal or the quality parameter.

3. The electrical test circuit according to claim 2, characterized in that the quality parameters are the standard deviation of the test signal and/or the deviation of the test signal and/or the amplitude of the test signal.

4. The electrical test circuit according to one of claims 1 to 3, characterized in that the test signal, the reference signal, the difference signal and the quality parameter or parameters are present in digital form.

5. The electrical test circuit according to one of claims 1 to 4, characterized in that from the difference signal and/or from the quality parameter, the ratio between the signal and the noise component (SNR) of the test signal and/or the ratio between the signal and the noise and/or distortion component (SNDR) of the test signal and/or the total unadjusted error (TUE) of the test signal and/or the total adjusted error (TAE) is/are calculated.

6. The electrical test circuit according to one of claims 1 to 5, characterized in that the control device (55) comprises a control loop circuit (501-507) which is provided for adapting the deviation of the test signal, the control loop circuit (501-507) being constructed in such a manner that a deviation-corrected test signal is generated in that the difference values between the deviation of the test signal and of the reference signal is added together and in that the test signal is corrected by addition with this aggregate difference value.

7. The electrical test circuit according to one of claims 1 to 6, characterized in that the control device (55) comprises an amplitude correction circuit (507-511) which is provided for matching the amplitude of the reference signal to the amplitude of the test signal, the amplitude correction circuit (507-511) being constructed in such a manner that an amplitude-corrected reference signal is generated in that the absolute value of the deviation-corrected test signal is determined and added together by the amplitude

correction circuit and in that the reference signal is corrected with the aggregate absolute value of the deviation-corrected test signal.

8. The electrical test circuit according to one of claims 1 to 7, characterized in that the control device (55) comprises a phase displacement circuit (6), the phase displacement circuit (6) being constructed in such a manner that the phase of the reference signal is matched to the phase of the test signal.

9. The electrical test circuit according to claim 8, characterized in that the phase displacement circuit (6) comprises a shift register (601), a decoder (602), at least one bus driver (603) and at least one D-type flip flop (604).

10. The electrical test circuit according to claim 8 or 9, characterized in that the phase of the reference signal is displaced up to one half signal period by the phase displacement circuit (6).

11. The electrical test circuit according to one of claims 1 to 10, characterized in that the squares of the amounts of the difference values between the deviation-corrected test signal and the amplitude- and phase-corrected reference signal is added together by the measuring device (56) and/or the minimum and maximum values of the difference values between the deviation-corrected test signal and the amplitude- and phase-corrected reference signal is stored by the measuring device (56).

12. The electrical test circuit according to claim 11, characterized in that the electrical test circuit is constructed in such a manner that the standard deviation is calculated by the measuring device (56) from the square of the amounts of the difference values

between the deviation-corrected test signal and the amplitude- and phase-corrected reference signal or from the minimum value of the difference values between the deviation-corrected test signal and the amplitude- and phase-corrected reference signal or from the maximum value of the difference values between the deviation-corrected test signal and the amplitude- and phase-corrected reference signal.

13. The electrical test circuit according to claim 11 or 12, characterized in that the electrical test circuit is constructed in such a manner that the phase of the reference signal is adjusted in accordance with the minimum of the standard deviation by the phase displacement circuit (6).

14. An electrical phase displacement circuit for correcting the phase of a reference signal with respect to a test signal of an integrated circuit, the electrical phase displacement circuit (6) having the following features:

- a first input (61), which is intended for receiving a reference signal from a tester (2),
- a second input (62) which is intended for receiving a clock pulse signal from a tester (2),
- at least one bus driver (603) which is connected to at least one D-type flip flop (604),
- the D-type flip flop or flip flops (604) are provided for displacing the phase of the reference signal,
- a shift register (601) and a selection element (602) connected to the shift register (601), particularly a decoder (602), which is formed in such a manner that in each case one bus driver (603) is activated in dependence on the data stored in the shift register (601),

- a first output (63) connected to the bus drivers (603), which is intended for sending out the phase-displaced reference signal,
- a second output (64) which is intended for sending out a control signal.

15. An electrical circuit for the tolerance tube test of integrated circuits, particularly of dynamic A/D converters, the electrical circuit (4) comprising an electrical test circuit (5) as claimed in one of claims 1 to 12 and an electrical phase displacement circuit (6) as claimed in claim 13, the first output (63) of the electrical phase displacement circuit (6) being connected to the third input (53) of the electrical test circuit (5) and the second output (64) of the electrical phase displacement circuit (6) being connected to the second input (52) of the electrical test circuit (5).

16. An integrated circuit comprising an electrical test circuit (5) according to one of claims 1 to 13 and/or with an electrical phase displacement circuit (6) of claim 13.

17. A probe card for testing integrated circuits, the probe card comprising an electrical test circuit (5) according to one of claims 1 to 13 and/or an electrical phase displacement circuit (6) of claim 14.

18. Load board for receiving a probe card for testing integrated circuits and/or with one or more test sockets for testing integrated circuits and/or for connecting a handler to a tester of integrated circuits, the load board comprising an electrical test circuit (5) according to one of claims 1 to 13 and/or an electrical phase displacement circuit (6) according to claim 14.

19. A tester with measuring sensors, particularly for currents and voltages, and with instruments for generating digital signals or data streams, the tester comprising one (2) electrical test circuit (5) according to one of claims 1 to 13 and/or an electrical phase displacement circuit (6) of claim 14.

20. The tester according to claim 19, characterized in that a low-pass filter (21) is provided which is constructed in such a manner that the digital signal received by the low-pass filter (21) or, respectively, the digital data stream received by the low-pass filter (21) is converted into an analog signal.

21. A tester with measuring sensors, particularly for currents and voltages, and with instruments for generating analog signals, the tester (2) comprising an electrical test circuit (5) according to one of claims 1 to 13 and/or an electrical phase displacement circuit (6) according to claim 14.

22. A method for testing an integrated circuit, comprising the following steps:

a) equipping a tester (2) with an integrated circuit (3),

b) applying current and voltage values to the integrated circuit (3) by the tester (2),

c) generating a reference signal by means of the tester (2), which corresponds to the ideal output signal of the integrated circuit (3),

d) displacing the phase of the reference signal in such a manner that the reference signal and the test signal of the integrated circuit (3) vary essentially synchronously,

e) matching the amplitude of the reference signal to the amplitude of the test signal,

f) matching the deviation of the test signal to the reference signal,

g) forming a difference signal by subtracting the reference signal from the test signal,

h) evaluating the difference signal.

23. The method as claimed in claim 22, characterized in that steps d) to g) are performed with an electrical test circuit (5) according to one of claims 1 to 13 and/or with an electrical phase displacement circuit (6) according to claim 14.

24. The method according to claim 22 or 23, characterized in that the electrical test circuit (5) and/or the tester (2) forms in step h) a quality value, particularly the standard deviation of the test signal and/or the deviation of the test signal and/or the amplitude of the test signal.

25. The method according to one of claims 22 to 24, characterized in that after step h) the electrical test circuit (5) and/or the tester (2) determine the ratio between the signal and the noise component (SNR) and/or the ratio between the signal and the noise and/or distortion component (SNDR) and/or the total unadjusted error (TUE) and/or the total adjusted error (TAE).

26. The method according to one of claims 22 to 25, characterized in that analog current and voltage values are applied to the integrated circuit (3) by the tester (2) in step b).

27. The method according to claim 26, characterized in that the tester (2) additionally comprises a conversion unit (21), particularly a low-pass filter (21), which, in step b), converts a digital data stream generated by the tester (2) into analog current and voltage values and applies these to the integrated circuit (3).

28. A computer program for executing a method for testing an electronic component, which is constructed in such a manner that the method steps b) - h) are executed according to one of claims 22-27.

29. The computer program as claimed in claim 28, which is contained on a storage medium, particularly in a computer memory or in a random access memory.

30. The computer program as claimed in claim 28 which is transmitted on an electrical carrier signal.

31. A data medium with a computer program as claimed in claim 28.

32. A method in which a computer program as claimed in claim 28 is downloaded from an electronic data network such as, for example, from the Internet to a computer connected to the data network.